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REMARKS

Claims 1-39 are pending in the present application. By this Response, claims 1, 14 and 27 are amended. Claims 1 and 14 are amended to recite a method or apparatus, respectively, "in a data processing system for creating instruction bundles". Claim 27 is amended and claims 1 and 14 are further amended to recite subject matter similar to "automatically determining a number of each possible type of instruction in the one or more instructions of the instruction group and dynamically creating one or more instruction bundles based on the number of each possible type of instruction in the one or more instructions of the instruction group". Reconsideration of the claims in view of the above amendments and following remarks is respectfully requested.

Amendments are made to the specification to correct errors and to clarify the specification. No new matter has been added by any of the amendments to the specification.

I. Examiner Interview

Applicants thank Examiner Tsai for the courtesies extended Applicants' representatives during the March 16, 2004 telephone interview. During the interview, Examiner Tsai indicated that the above amendments would overcome the Hull reference. Therefore it is Applicants understanding that, pending an update search by Examiner Tsai, the present claims are now in condition for allowance. The substance of the interview is summarized in the remarks of Section II, which follows.

II. 35 U.S.C. § 102, Alleged Anticipation, Claims 1-39

The Office Action rejects claims 1-39 under 35 U.S.C. § 102(b) as being allegedly anticipated by Hull et al. (U.S. Patent No. 5,922,065). This rejection is respectfully traversed.

As to claims 1, 14 and 27, the Office Action states:

Hull et al. discloses as claimed, a method for creating instruction bundles (comprising slot0, slot1 and slot2, see Fig. 4), comprising: receiving an instruction group (see Col. 4, lines 1-2) having one or more instructions (comprising the instruction types in the table 20 as shown in Fig. 2); determining a number of each possible type of instruction in the one or more instructions of the instruction group limitations (see Fig. 4, the instructions are grouped into different groups separated by the double lines 42 and 43; and the stop bits (S-bit see Fig. 2), see also Col. 4, lines 43-45, and lines 61-67, each group comprises different execution unit types, such as I-unit, M-unit, and F-unit see Figs. 2 and 4 based on the architectural limitations thereof); and creating one or more instruction bundles (comprising slot0, slot1 and slot2, see Fig. 4) based on the number of each possible type of instruction in the one or more instructions of the instruction group (as set forth above, see Fig. 4) based on the number of each possible type of instructions in the one or more instructions of the instruction group (as set forth above, see Fig. 4, the instructions are grouped into different groups separated by the double lines 42 and 43; and the stop bits (S-bit see Fig. 3), see also Col. 4, lines 43-45, and lines 61-67, each group comprises different execution unit types, such as I-unit, M-unit, and F-unit see Figs. 2 and 4 based on the architectural limitations thereof).

Office Action dated January 2, 2004, pages 3-4.

Claim 1, which is representative of the other rejected independent claims 14 and 27, with regard to similarly recited subject matter reads as follows:

1. A method for creating instruction bundles, comprising:
receiving an instruction group having one or more instructions;
determining a number of each possible type of instruction in the one or more instructions of the instruction group; and
creating one or more instruction bundles based on the number of each possible type of instruction in the one or more instructions of the instruction group.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. In re Bond, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. In re Lowry, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983).

Applicants respectfully submit that Hull does not identically show each and every feature of the claims arranged as they are in the claims. Specifically, Hull does not teach determining a number of each possible type of instruction in the one or more instructions of the instruction group and creating one or more instruction bundles based on the number of each possible type of instruction in the one or more instructions of the instruction group.

Hull is directed to a processor having a large register file that utilizes a template field for encoding a set of the most useful instruction sequences in a long instruction word format. The instruction set of the processor includes instructions which are one of a plurality of different instruction types. The execution units of the processor are similarly categorized into different types, where each instruction type may be executed on one or more of the execution unit types. The instructions are grouped together into 128-bit sized and aligned containers called bundles, with each bundle includes a plurality of instruction slots and a template field that specifies the mapping of the instruction slots to the execution unit types.

Thus, with the system of Hull, instruction sequences are encoded into a long instruction word format using a template field. Each instruction sequence is categorized into an execution unit type, which are then grouped together into bundles. The bundles include a plurality of instruction slots and a template field that specifies the mapping of the instruction slots to the execution unit types. There is no teaching anywhere in the Hull reference as to determining a number of each possible type of instruction in the one or more instructions of the instruction group. The Office Action alleges that this feature is taught at Figures 2 and 4, column 4, lines 43-45 and column 4, lines 61-67, which are reproduced below:

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INSTRUCTION TYPE	DESCRIPTION	EXECUTION UNIT TYPE
A	INTEGER ALU	I-UNIT OR M-UNIT
I	NON-ALU INTEGER	I-UNIT
M	MEMORY	M-UNIT
F	FLOATING POINT	F-UNIT
B	BRANCH	B-UNIT
L	LONG IMMEADIATE	I-UNIT

FIG. 2

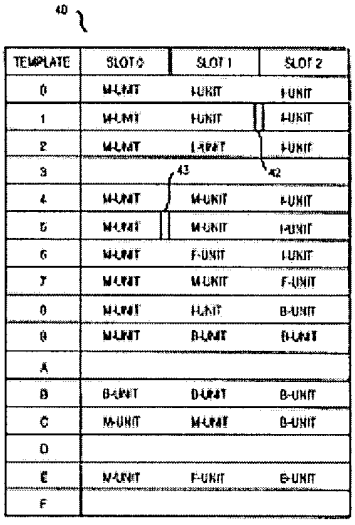

FIG. 4

Note that table 40 includes double lines 42 and 43 separating two instruction slots associated with template 1 and template 5, respectively.

(Column 4, lines 43-45)

Within a bundle, execution order proceeds from slot 0 to slot 2. If the S-bit is 0, the instruction group containing the last instruction (slot 2) of the current bundle continues into the first instruction (slot 0) of the statically next sequential bundle. On the other hand, if the S-bit is 1 an instruction group boundary occurs after the last instruction of the current bundle.

(Column 4, lines 61-67)

In Figure 2, Hull is showing the relationship between the instruction types and the execution unit types. In Figure 4, Hull is showing the template field encoding and instruction slot mapping for the processor. In column 4, lines 42-45, Hull is describing the double lines that separate two instruction slots within the template. In column 4, lines 61-67, Hull is describing the execution order process within the template. There is nothing in these figures and sections, or any other figure or section of Hull, which teaches determining a number of each possible type of instruction in the one or more instructions of the instruction group. The system of Hull merely loads the instruction sequence into a template, which is then bundled together into 128-bit sized bundles. There is no counting or any other operation performed which would result in the number of each possible type of instruction being determined within the group of instructions. Hull simply is not concerned with determining the number of each possible type of instruction in the instructions of the instruction group.

Furthermore, Hull does not teach creating one or more instruction bundles based on the number of each possible type of instruction in the one or more instructions of the instruction group. As discussed above, Hull is not concerned with determining the number of each possible type of instruction in the instructions of the instruction group. Hull is only concerned with bundling instruction together based on instructions that are 128 bits in size. The Office Action alleges that this feature is taught at Figures 2 and 4, column 4, lines 43-45 and column 4, lines 61-67, shown above. As discussed above, these figures and sections merely show and describe the relationship between the instruction types and the execution unit types, the template field encoding and instruction slot mapping for the processor, the double lines that separate two instruction slots within the template and the execution order process within the template. While Hull may teach bundling, the bundling is based only on instructions that are 128 bits in size and not based on the number of each possible type of instruction in the one or more instructions of the instruction group. In other words, the bundling in Hull is performed in a completely different manner from that of the claimed invention.

Thus, Hull does not teach each and every feature of claims 1, 14 and 27 as is required under 35 U.S.C. § 102(b). At least by virtue of their dependency on independent claims 1, 14 and 27, respectively, Hull does not teach each and every feature of

dependent claims 2-13, 15-26 and 28-39. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 1-39 under 35 U.S.C. § 102(b).

Furthermore, Hull does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. Absent the Examiner pointing out some teaching or incentive to implement Hull to determine the number of each possible type of instruction in the one or more instructions of the instruction group and create one or more instruction bundles based on the number of each possible type of instruction in the one or more instructions of the instruction group, one of ordinary skill in the art would not be led to modify Hull to reach the present invention when the reference is examined as a whole. Absent some teaching, suggestion, or incentive to modify Hull in this manner, the presently claimed invention can be reached only through an improper use of hindsight using the Applicants' disclosure as a template to make the necessary changes to reach the claimed invention.

Moreover, in addition to their dependency from independent claims 1, 14 and 27, respectively, Hull does not teach the specific features recited in dependent claims 2-13, 15-26 and 28-39. For example, with regard to claims 10, 23 and 36, Hull does not teach determining a number of each possible type of instruction in the one or more instructions of the instruction group includes incrementing instruction counters based on the number of each possible type of instruction in the one or more instructions, and wherein creating one or more instruction bundles includes decrementing the instruction counters as instructions are added to instruction bundles. The Office Action alleges that these features are taught at column 5, lines 15-23, which reads as follows:

> Bundles are ordered from lowest to highest memory address. Instructions in bundles with lower memory addresses are considered to precede instructions in bundles with higher memory addresses.
>
> The byte order of bundles in memory is little-endian. This means that the template field and the S-bit are contained in byte 0 of the bundle. Within a bundle, instructions and instruction groups are ordered from instruction slot 0 to instruction slot 2 as shown in FIG. 3.

In this section, Hull is describing bundles are ordered such that bundles with lower memory addresses are considered to precede instructions in bundles with higher memory addresses. Nowhere in this section, or any other section of Hull, are instruction counters incremented based on the number of each possible type of instruction in the one

or more instructions or are instruction counters decremented as instructions are added to instruction bundles. In fact, this section has nothing to do with actually bundling instruction but instead is directed to how bundles are stored in memory relative to other bundles. Moreover, nowhere is a counter even mentioned in this or any other section of Hull, let alone incrementing/decrementing counters in the manner recited.

As an additional example, with regard to claims 6-9, 11-13, 19-22, 24-26, 32-35 and 37-39, Hull does not teach creating instruction bundles based on anything other than the bundle being 128 bits in size. Hull teaches that instructions execution order proceeds from slot 0 to slot 2, within the template and if the S-bit is 0, the instruction group containing the last instruction (slot 2) of the current bundle continues into the first instruction (slot 0) of the statically next sequential bundle and if the S-bit is 1 an instruction group boundary occurs after the last instruction of the current bundle, (see column 4, lines 61-67). Thus, the instructions are bundled together based upon how they appear within the template in 128-bit sized bundles. Nowhere, in any section of Hull, is it taught that instructions are taken in order of their flexibility in terms of where that instruction can be placed in the available bundle types, as in claims 6, 19 and 32; creating one or more instruction bundles is performed based on a most common instruction combination first, as in claims 7, 20 and 33; creating one or more instruction bundles is performed based on a most restrictive instruction type placement and proceeds to less restrictive instruction type placement second as in claims 8, 21 and 34; creating one or more instruction bundles is performed based on a most restrictive instruction type placement and proceeds to less restrictive instruction type placement, as in claims 9, 22 and 35; where the most common instruction combination is where all instructions in the instruction group are of a memory instruction type, integer instruction type or integer arithmetic logic unit type, as in claims 11, 24 and 37; where creating one or more instruction bundles includes ensuring that creating the one or more instruction bundles does not introduce hardware oversubscription, as in claims 12, 25 and 38; or ensuring that creating the one or more instruction bundles does not introduce hardware oversubscription includes forming partial instruction bundles, as in claims 13, 26 and 39.

Therefore, in addition to being dependent on independent claims 1, 14 and 27, respectively, dependent claims 2-13, 15-26 and 28-39 are also distinguishable over Hull

by virtue of the specific feature recited in these claims. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 2-13, 15-26 and 28-39 under 35 U.S.C. § 102(b).

III. Conclusion

It is respectfully urged that the subject application is patentable over the prior art of record and is now in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

Respectfully submitted,

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